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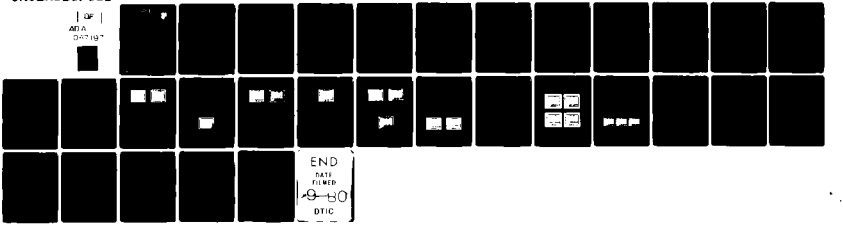

LEVEL II

(13)

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Interim Report
February 1980

DESIGN, FABRICATION AND TEST OF A CCD-BASED CORRELATOR/CONVOLVER

Raytheon Company

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Tests conducted since the first interim report have emphasized the characterization of the elements of the correlator/convolver, rather than the performance of the complete device. Prior work having vindicated the choice of the four transistor bridge configuration, the present interim period focused on the adequacy of the floating gate and source followers as designed. An extensive characterization of the floating-gate-output CCD test pattern was carried out.

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Maximum signal swing, linearity and noise level were measured with four different input techniques. All results were as good or better than expected. Accuracy of about one percent could be maintained over a signal range of about 4.25 volts. Surprisingly, the potential equilibration techniques gave linearity at least as good as that obtained with the diode-cutoff method. However, the potential equilibration input was up to 15 dB quiter. The signal to noise ratio referenced to the 1% nonlinearity signal level was approximately 80 dB, 10 dB better than the design goal. With the additional 6 dB enhancement of signal over noise of the bridge multiplier as compared to conventional multiplier designs, a net effective input signal to noise ratio of about 85 dB is expected in the complete correlator/convolver. Finally, the design of the deliverable 256-stage correlator was completed and entered into the maskmaking CAD system. The problem reported earlier with direct feedthrough of the drain inputs was found to be due to a difference in characteristics between transistors located under one and under two layers of polysilicon and will be corrected in this final design. The final chip size will be 8.7 mm by 3.25 mm and with 4128 CCD cells and 4132 transistors represents one of the first analog integrated circuits that is truly on the scale of a digital LSI device.

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1. INTRODUCTION

The purpose of this program is the development of a CCD-based correlator/convolver suitable for use in advanced USAF military electronic systems.

The specific objective of this program is to fabricate and deliver 20 best effort samples of CCD-based correlator/convolver devices aimed at the design goals listed in Table 1.

TABLE 1. OVERALL PERFORMANCE GOALS

CCD Dynamic Range	60 dB 70 dB after input normalization
CCD Clock Rate	32 kHz to 10 MHz at 25°C 500 kHz to 10 MHz at +85°C
CCD Size	256 Stages
Relative correlation error (percent of theoretical for pulse waveforms w/25 percent duty cycle)	1 percent
Power Dissipation	300 mW

The performance goals outlined above were selected to meet or exceed contract requirements.

The first interim report described earlier work completed, in process, and planned under the contract. It began with a discussion and analysis of design tradeoffs and followed with a description of the process design and mask design used for the first generation test mask series. Later, test pattern results were reviewed and plans for the second phase of the program were described.

The tests conducted since the first interim report have continued to emphasize the characterization of the elements of the correlator/convolver, rather than the performance of the complete device.

Since prior work put a heavy emphasis upon the characterization of the multipliers and led to a vindication of the choice of the four transistor bridge configuration, it remained to determine the adequacy of the floating gate and source followers as designed. An extensive characterization of the floating-gate-output CCD test pattern was carried out. Maximum signal swing, linearity, and noise level were measured with four different input techniques. Two of these input techniques used the gated-diode or diode-cutoff sampling method; the other two used potential equilibration.

All of the results were as good as or better than expected. The maximum output signal swing with 8 V of clock amplitude for the general clocks and 14 V for the floating gates was nearly 6 V. Accuracy of about 1 percent could be maintained over a signal range of about 4-1/4 V. Surprisingly, the potential equilibration input techniques gave linearity at least as good as that obtained with the diode-cutoff method. The noise levels, however, were very different, the potential equilibration input being up to 15 dB quieter. The signal-to-noise ratio referenced to the 1 percent nonlinearity signal level was approximately 80 dB, 10 dB better than our goal. Since the bridge multiplier provides an additional 6 dB enhancement of signal over noise as compared to conventional multiplier designs, a net effective input signal-to-noise ratio into the multipliers of approximately 85 dB can be expected in the complete correlator/convolver.

A new method for interfacing the output of the correlator/convolver was also investigated using a RAYCAP computer circuit simulation program. It is also described in the pages which follow.

In addition to the above work, the design of the deliverable 256-stage correlator was also completed and entered into the mask-making CAD system. The design features of the final configuration are also discussed in the sections which follow.

This report ends with a discussion of conclusions and plans for the next reporting period.

2. FLOATING GATE STUDIES

2.1 Chip Schematic and Input Techniques

A partial schematic diagram of the floating-gate CCD test pattern chip is shown in Figure 1. The CCD has a total os six stages, the second through fifth of which have floating-gate output taps as shown. In addition, the CCD has a dual channel, so that the circuit of Figure 1 really occurs twice in parallel. For the experiments performed here, the diffusions (CCD-S and CCD-D), input gates (IG1 and IG2), clock phases (ϕ1, ϕ2, ϕ3, ϕ4, and ϕc), and the source follower bias lines (V_{DD}, V_{GG}, and V_{SS}) were connected in parallel.

The three elements of the input structure—CCD-S, IG1, and IG2— were used in four different ways to control the conversion of input voltage to CCD charge. Two of them are shown in Figure 2. Both use equilibration of the channel potentials under IG1 and IG2 to meter the charge. The negative-going sampling pulse SP on the CCD source diffusion (CCD-S) initially overfills the input well under IG2. The charge injected into the CCD is given by Equation (1) provided $V_{IG2} \geq V_{IG1}$. If $V_{IG2} < V_{IG1}$, Q=0. Also, as V_{IG2} approaches the high level of the clocks, the value of Q saturates. The coefficient C_{oxide} is the oxide capacitance of the IG2 electrode. The charge consists of electrons; hence Q is negative.

$$Q = -C_{oxide} (V_{IG2} - V_{IG1}) \qquad (1)$$

Since the constant oxide capacitance appears in this expression, the conversion of input voltage to charge is expected to be highly linear. This does not necessarily mean that the best overall device linearity will result, since the floating gate sensing may not be linear.

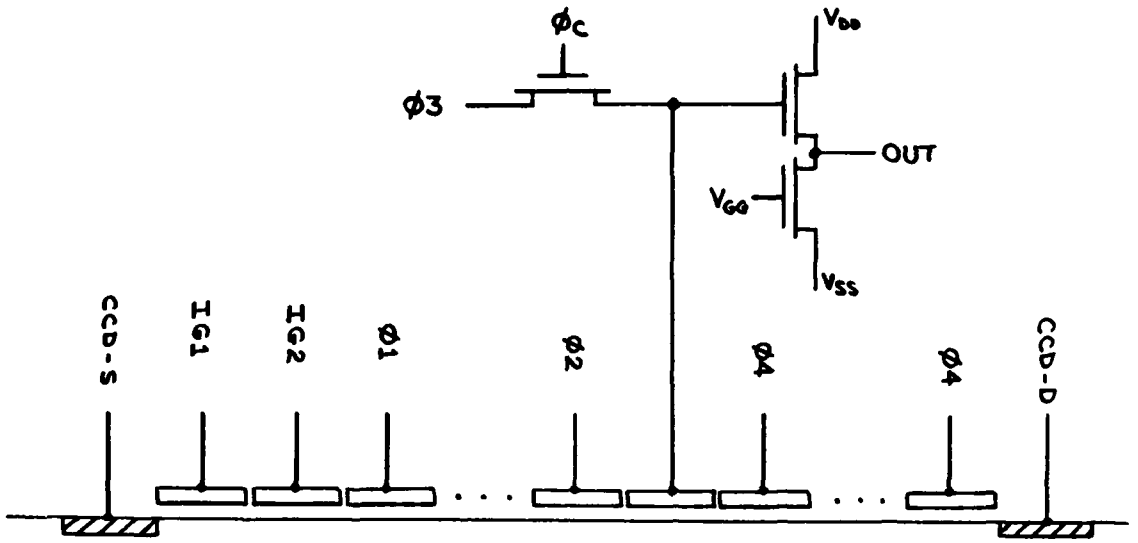

Figure 1. Partial Schematic Diagram of Floating Gate CCD Test Chip

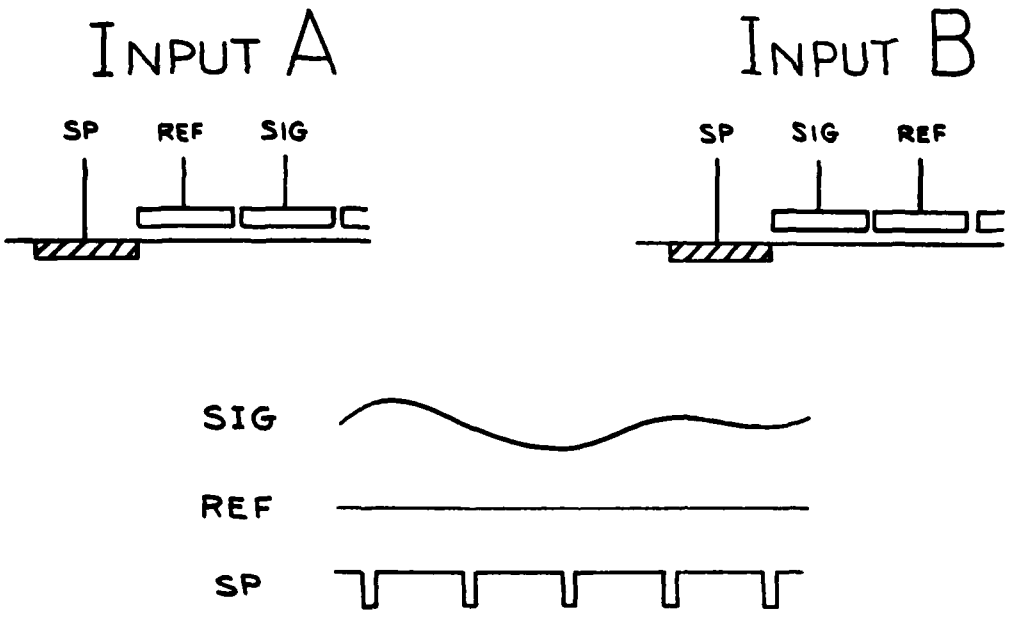

Figure 2. Two-Charge Equilibration Type Input Techniques

The two gated diode type inputs are shown in Figure 3. Input D should obey Equation (1) with V_{IG1} replaced by the value of IG1 voltage that would produce a channel potential equal to the reference voltage applied to the CCD source. Input C obeys an equation of the form given in Equation (2).

$$\frac{dQ}{dV_{SIG}} = C_{oxide} + C_{DEPL}(V) \qquad (2)$$

The capacitance that controls the ratio of incremental charge to incremental signal voltage includes the depletion capacitance C_{DEPL} under IG2. Since this capacitance depends on the signal voltage, a nonlinear relationship between charge and voltage is expected.

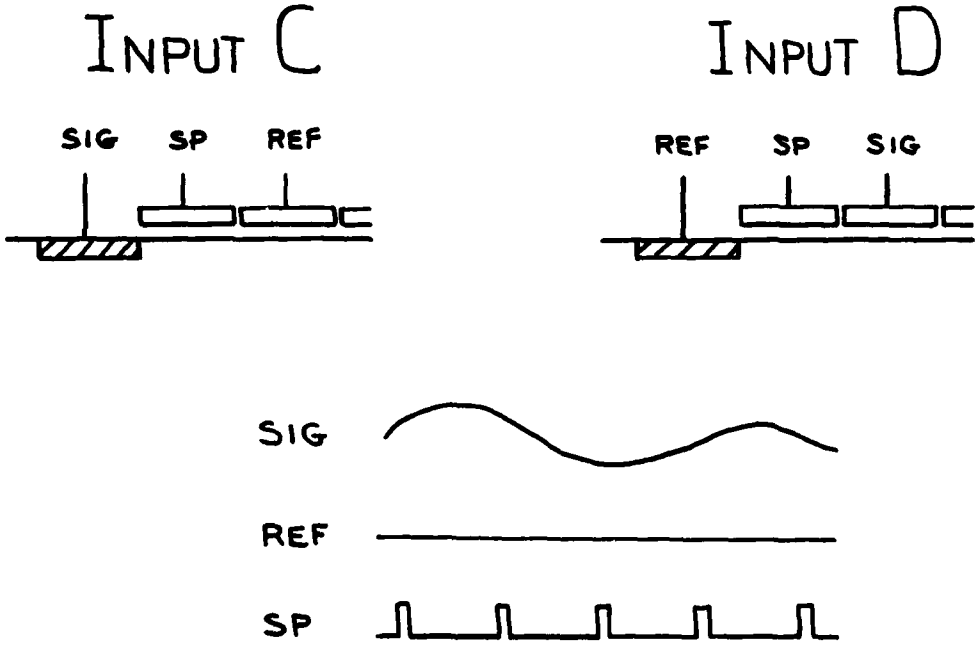

Figure 3. Two-Gated Diode Type Input Techniques

2.2 Test Fixture

The experiments reported on here were performed on a complete un-diced wafer using a wafer probe station with a probe card. Poor matching conditions and high capacitance between probes limits the frequency at which measurements can be made. Laboratory pulse generators with 50 Ω back-matched outputs provided the clocking waveforms. Digitally-set power supplies with by-pass capacitors on the probe card connector furnished low-noise dc levels.

The major speed limitation is determined by the drive capability of the output source followers. The load capacitance of the scope probe and probe card was estimated to be about 20 pF. With the source follower load current set to 20 μA, the downward slewing rate is only 1 V/μsec. The on-chip load in the correlator will be at least 20 times smaller.

2.3 Absolute Calibration

Measurement of the outputs from the floating gate taps gives no information about the absolute size of the charge packets in the CCD. To provide such information, the CCD was set up with conventional four-phase overlapping clocks operating at 0.1 MHz. The control phase ϕc was held at a high dc bias so that the phase 3 gates were never floating. By measuring the average current flowing from the CCD drain (CCD-D) at the known clock frequency, we could calculate the size of the charge packets. Data obtained using the potential equilibration input technique are shown in Figure 4. The slope of the curves gives a value of 1.1 pF for the oxide capacitance under IG2. The value actually varies by 2 to 3 percent depending on the bias on IG1.

As found from the results described in Subsection 2.5, the peak input swing on IG2 for linearity within 1 percent is about 3 V. This corresponds to a maximum signal charge packet of 3.3 pC or 20 million electrons. Shot noise for such a charge packet would be about 4500 electrons, 73 dB below the signal. The KTC noise on the input capacitor would be about 400 electrons, 94 dB below the signal.

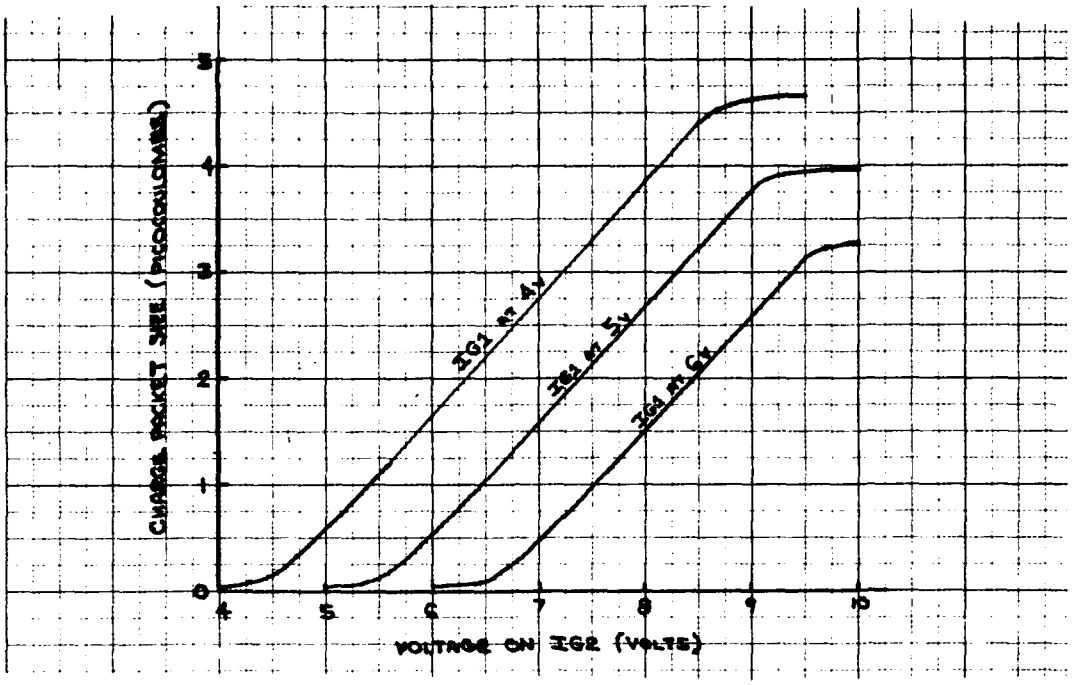

Figure 4. Charge Packet Size for Potential Equilibration Input

2.4 Clock and Output Waveforms

Clock and output waveform timing for four-phase operation is shown in Figure 5. The polarity of SP depends on the input technique in use. Two versions of the actual outputs are shown in Figure 6. In both cases $\phi 1$, $\phi 2$, and $\phi 4$ went from 2 V to 10 V. For Figure 6a, $\phi 3$ went from 2 V to 12 V and ϕc from 6 V to 13 V. The source follower biases were V_{SS} = 4.5 V, V_{GG} = 7.0 V, and V_{DD} = 10 V, and the drain current was 20 μA per source follower. The bottom line in the photo is +4 V. In Figure 6b, $\phi 3$, ϕc, V_{SS}, and V_{DD} were adjusted to give the maximum possible signal swing of just under 6 V. The high level of $\phi 3$ was increased to 14.5 V, and ϕc went from 7.5 V to 15 V. The source follower load current was reduced to emphasize the slewing rate limit on negative-going output transitions. An 8.5 V difference between V_{DD} and V_{SS} was required for the 6 V signal swing; a difference of 5.5 to 6 V was adequate for a 4 V signal swing.

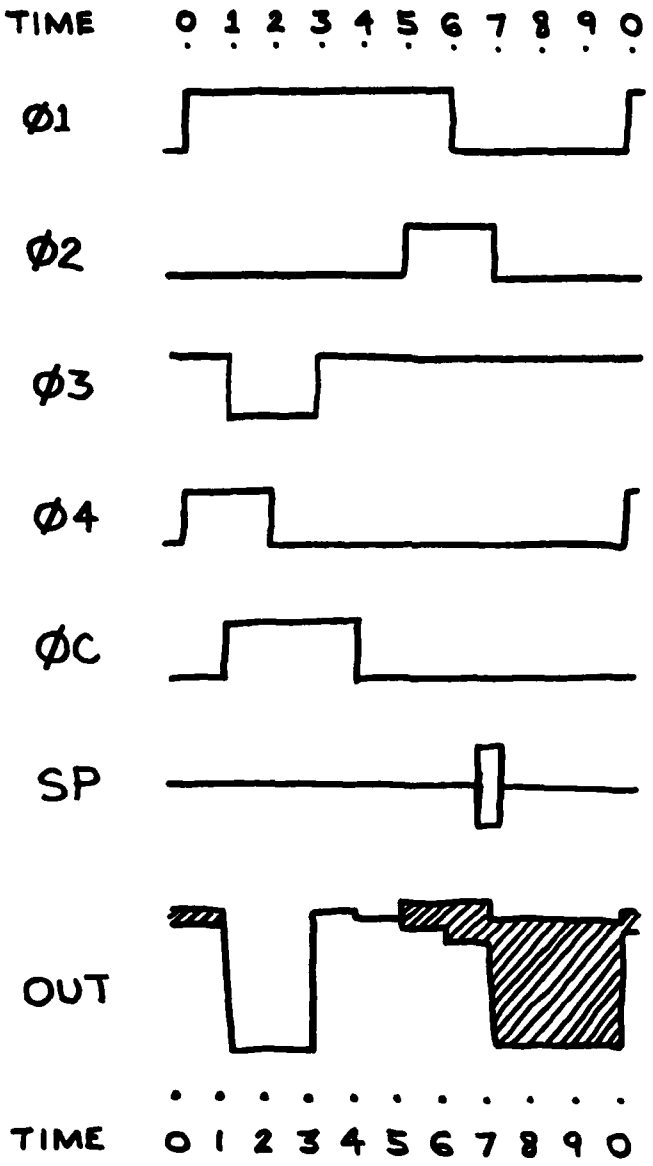

Figure 5. Diagram Showing Clock and Output Timing

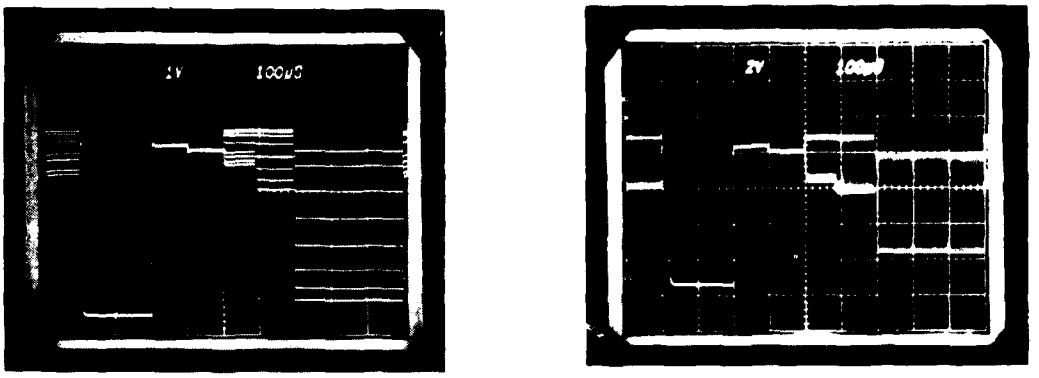

Figure 6. Examples of Actual Output Waveforms With CCD Operating at a Clock Frequency

The various parts of the output waveform are explained as follows. From time 1 to 4 the output gates are not floating but rather are driven by $\phi 3$. When $\phi 3$ is low during the time interval from 1 to 3 the output is saturated at V_{SS}. During the time interval from 4 to 5 the gate is floating, but no charge has entered the gate region since $\phi 2$ is still low. The slight negative step at time 4 is presumably due to capacitive feedthrough of the negative ϕc transition. When $\phi 2$ goes high at time 5 capacitive coupling due to clock electrode overlap drives the floating gate more positive and allows the signal charge to spread under the $\phi 1$, $\phi 2$ and $\phi 3$ (FG) gates. At time 6, $\phi 1$ goes low, forcing the signal charge into the $\phi 2$ - $\phi 3$ region. Finally at time 7, when $\phi 2$ returns low, all of the signal charge is forced under the floating gate $\phi 3$, and the full signal appears on the output. At time 0 phases 4 and 1 turn on, again allowing the signal charge to spread under three gates ($\phi 3$, $\phi 4$, $\phi 1$).

2.5 Linearity

For studies of the linearity and noise levels, the time unit was reduced 200 times from 100 μsec to 0.5 μsec for the interval from 0 to 7 in Figure 5.

The overall clock period was reduced only 20 times to 50 μsec (fc = 20 kHz). In this way the interval during which a valid output occurs was increased from 30 percent to 93 percent of the clock cycle. The 7 percent of the time that contains an invalid signal is not visible on an oscilloscope trace.

Figure 7 shows the input and output waveforms for a slow, linear, triangle wave input signal. The output is displayed at 1 V per division and is inverted; the scale factor and dc level of the input signal were adjusted to bring the traces into close proximity for sensitive visual comparison. One can just barely determine that the traces track within 1 percent over an output signal swing of 4 V.

A faster and more sensitive measurement technique is to examine the output on a spectrum analyzer with a sine wave input. Figure 8 shows such an analysis for the CCD operating with input type A Figure 2. The photo on the left shows the spectral content of the 3 V peak-to-peak input signal (5 V to 8 V absolute) applied to IG2. The third harmonic is 50 dB down. The photo on the right shows the 4.5 V peak-to-peak output. The critical third harmonic is at -39 to -40 dB.

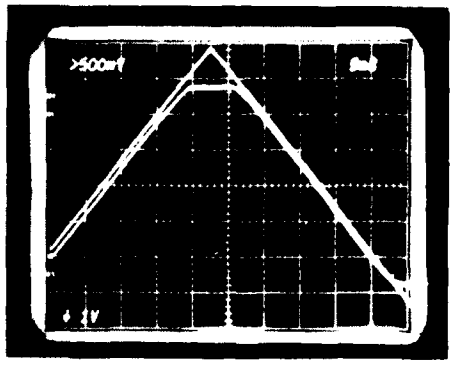

Figure 7. Comparison of Input and Output for a Linear Triangle Waveform

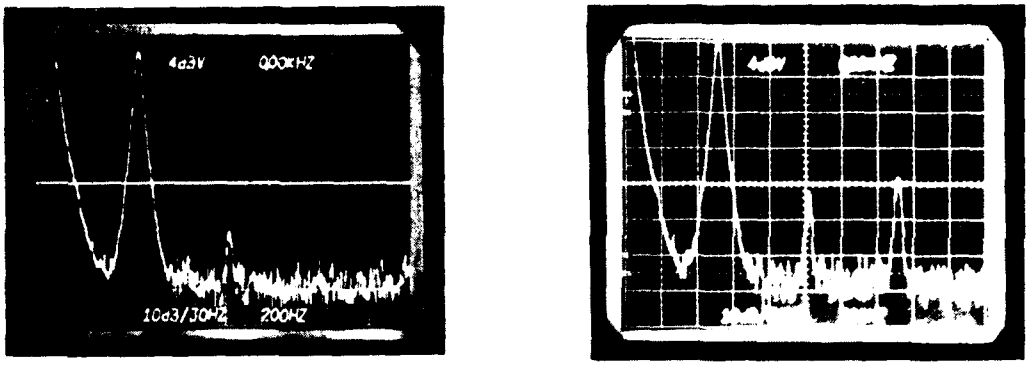

Figure 8. Spectral Analysis Using Input Technique A

The 40 dB level is the minimum sensitivity of the experiment as performed here. Reducing the amplitude of the input signal did not dramatically decrease the harmonic distortion relative to the signal peak as would be expected ordinarily. This is because the signal is valid over only 93 percent of the output time interval (actually a little less because of the time required for the output to slew to its final value). Of the 7 percent of the time when there is an invalid output, dc levels occur over 4 percent and spurious signal-related output over 3 percent. A back-of-the-envelope estimate of the third harmonic content introduced gives a value in the range -40 to -50 dB, consistent with what is observed experimentally. The experiment could be improved by using an external sample-and-hold circuit, though the accuracy is quite sufficient for the present purposes. If we want to extend the measurements to higher clock frequencies, the sample-and-hold will have to be used.

The harmonic response of input type B is shown in Figure 9. Gate IG2 was held at a bias of 7.3 V while the signal on IG2 ranged from 3.3 V to 6.2 V (2.9 V peak-to-peak). The output ranged from 5.7 V to 10.3 V (4.6 V peak-to-peak). Again the third harmonic is 39 to 40 dB down.

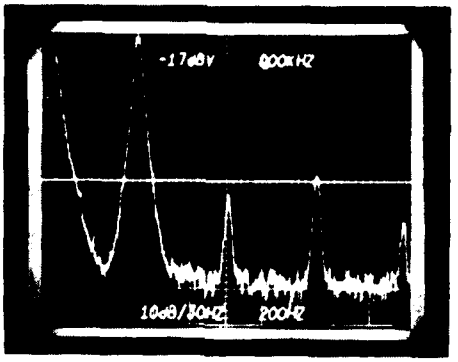

Figure 9. Spectral Response Using Input Type B

Signals using input type C are shown in Figure 10. The left photo shows the input and output waveforms, both at 2 V per division. The input on CCD-S goes from 3.35 V to 6.25 V (2.9 V peak-to-peak), and the output swing is from 5.6 V to 10.6 V (5.0 V peak-to-peak). The 250 μsec (5 x 50 μsec) delay from input to output due to five stages of CCD delay can be seen. The photo on the right shows third harmonic at about -38 dB for this very large output signal amplitude.

Figure 11 shows the spectral response for input type D. The CCD source was biased to 3.1 V dc, the input signal on IG2 swung from 3.8 V to 7.1 V (3.3 V peak-to-peak), and the output range was 5.6 V to 10.7 V (5.1 V peak-to-peak). Again the third harmonic is 38 dB down.

The general conclusion from these results is that any of the four input techniques can be used to produce adequately linear input voltage to output voltage transfer curves for output swings up to about 4 V peak-to-peak.

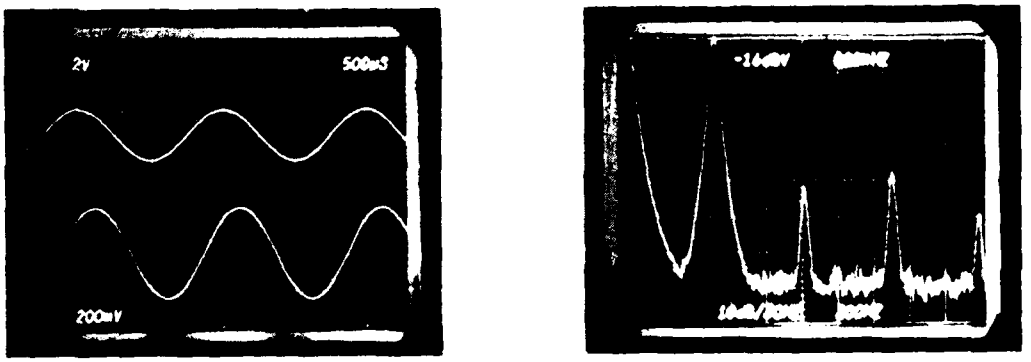

Figure 10. Response Using Input Type C

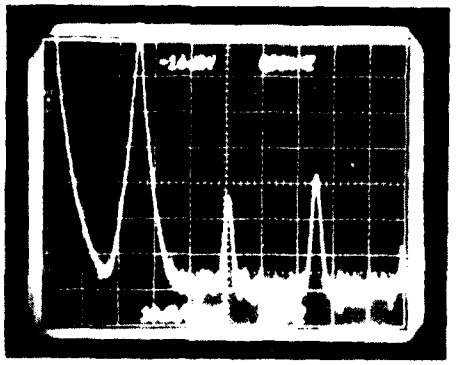

Figure 11. Spectral Response for Input Type D

2.6 Noise

The noise was measured for the two general types of input techniques. Figure 12 shows the noise spectrum out to the Nyquist frequency of 10 kHz in two bands for input type D. Integration of the noise power over the Nyquist band yields a signal-to-noise ratio (including the 2.5 dB correction factor for the averaging characteristics of the spectrum analyzer) of 65 dB. With the probe tip grounded, the noise level was 7 dB lower than that shown in Figure 12. Also, when the bias on IG2 was reduced to 1 V so that the input was cut off, the observed noise dropped to the analyzer noise floor level.

When a x1 probe was used to achieve greater sensitivity, the signal-to-noise ratios were found to be approximately 79 dB with the input cut off, 65 dB with IG2 at 4 V (small signal packet), and 68 dB with IG2 at 7 V (large signal packet). The dc biases on CCD-S and IG2 had noise levels at least 5 dB below the noise curve with the input cut off. The gated diode input operation was clearly responsible for the noise.

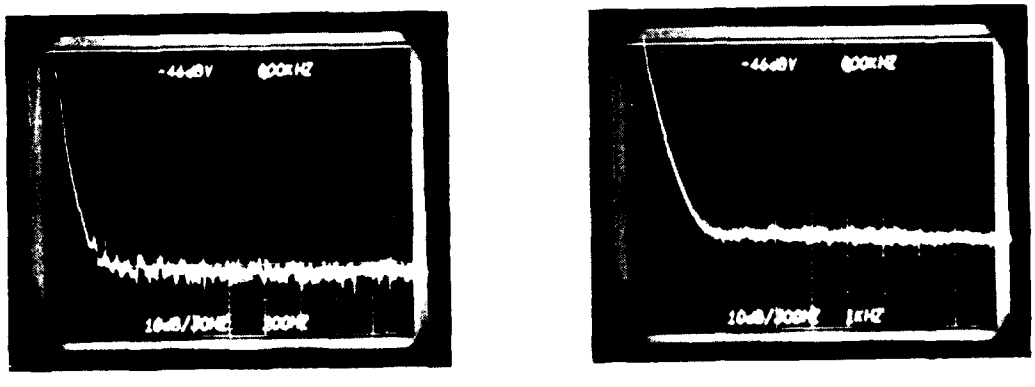

Figure 12. Noise Spectrum for Gated Diode Input with Nearly Full Charge Packets

The sampling pulse for the above experiments was 0.5 μsec long with 0.1 μsec rise and fall times. When the cutoff transition was lengthened to 2 μsec over the 4.5 V transition, the following improved signal-to-noise ratios were obtained: 76 dB with IG2 at 4 V, 73 dB with IG2 at 5 V, and 70 dB with IG2 at 7 V. Further lengthening of the SP transition had little if any effect.

Figure 13 shows the noise spectrum using potential equilibration input type A with a small signal present. In the upper left photo the signal has an amplitude of 2 V peak-to-peak. In the upper right photo, the signal amplitude has been reduced 20 dB and the analyzer sensitivity increased by 20 dB. A nonrandom noise peak is clearly visible at about 2.5 kHz. It was caused by transients riding on the dc power supply lines. The signal amplitude and analyzer sensitivity were changed by another 20 dB to get the lower left photo. Finally, the lower right photo shows the full Nyquist band (the signal frequency was doubled also). Integration of the noise power over the 10 kHz Nyquist band but excluding the coherent noise gave a signal-to-noise ratio of 81 dB.

We do not fully understand why the gated diode input is so noisy. Conventional thinking is that partitioning of the charge stored in the channel under IG1 contributes additional noise. This is undoubtedly true. However, that noise contribution could not exceed the shot noise for a full charge packet, which we calculated to be -73 dB in Subsection 2.3. Another source of noise relates to the input sampling bandwidth. The gated diode input provides a very narrow aperture that is capable of sampling a very high bandwidth signal. Consequently it is sensitive to the noise over a bandwidth beyond the Nyquist limit. It is the classic problem of providing more input bandwidth than the remainder of the device can use; the result is degraded signal-to-noise ratio. With a sampling pulse fall time of 0.1 μsec, one can expect noise on the input control structures over a bandwidth of 10 MHz to contribute to charge fluctuations in the packet. The thousand-to-one ratio (30 dB) of noise bandwidth to Nyquist frequency can result in significant noise contributions from signals whose spectral power density is very low.

The potential equilibration input technique, on the other hand, does not provide a precision sampling aperture. Input A tends to sample the minimum signal value and input B the maximum signal value in the interval between the

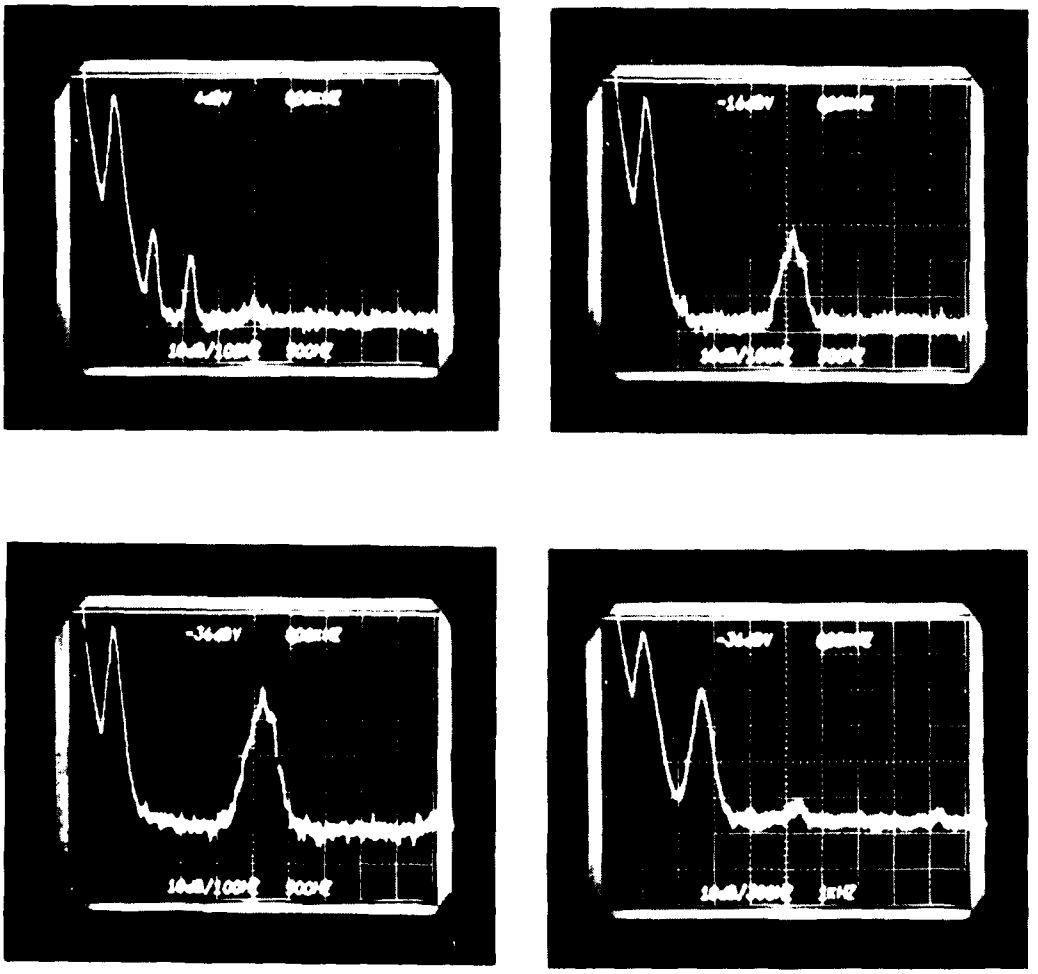

Figure 13. Noise Spectra Using Potential Equilibration Input Type A

end of the sampling pulse and when the charge enters the CCD shift register. As the equilibration progresses, the resistance of the channel under IG1 increases, increasing the RC time constant of the input. This limits the input bandwidth automatically.

While the slow sampling characteristic of the potential equilibration input improves its noise level, it can also result in inaccuracies, as shown by the photos in Figure 14. The CCD was operating at a clock frequency of 10 kHz with an input signal at 1 kHz, 20 percent of the Nyquist limit. The upper trace in the photos shows the position of the sampling pulse relative to the $\phi 1$ ON transition. In the left photo 80 μsec are allowed for equilibration, during which time the input signal can change by as much as 25 percent of its peak-to-peak swing. The second harmonic is only 22 dB down. In the middle photo the equilibration time has been reduced to 50 μsec, reducing the maximum possible signal change to 15 percent. The second harmonic has dropped 5 dB. In the final photo only 20 μsec is allowed for equilibration, and the signal cannot change by more than 6 percent during that time. The second harmonic is now at -38 dB.

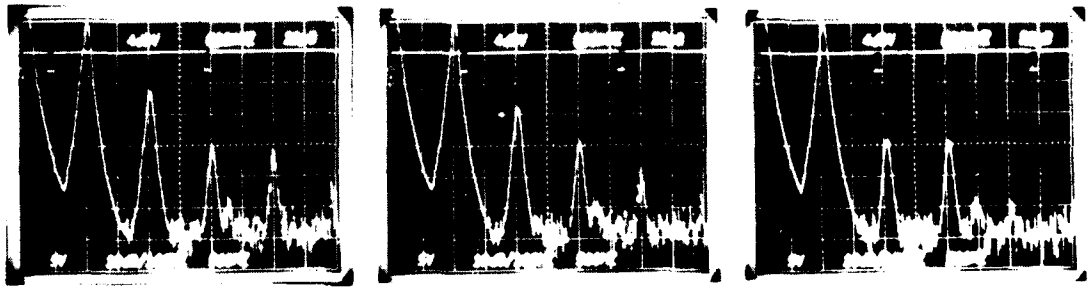

Figure 14. Sampling Error for Long Equilibration Times with Potential Equilibration Inputs

3. MULTIPLIER OUTPUT TECHNIQUE

The work reported in this section was not performed under the contract and does not relate specifically to the design of the correlator/convolver chip. It does, however, suggest a way in which the chip outputs can be processed and illustrates a further advantage of the bridge type multiplier cell.

Although we pointed out that the output current summing busses from a bridge multiplier array need not be held at any specific dc bias, we always assumed that they would be held at some bias, that each current would be converted to a voltage, and that the two voltages would be subtracted to yield the final result. This is not necessary. Consider the circuit shown in Figure 15. The bridge multiplier array is indicated schematically by the diamond shaped element. The output current busses, labelled $\Sigma+$ and $\Sigma-$, are connected to the primary of a transformer. The secondary of the transformer is effectively shorted by the operational amplifier. Consequently, the impedance between the current busses $\Sigma+$ and $\Sigma-$ is very low and they will remain at the same potential. The value of that potential is not imposed externally; instead, the busses will self-bias to a value that results in the currents in the two busses being at all times equal and opposite. Thus, the voltage on the busses may vary in time.

The RAYCAP circuit simulation program was used to study the performance of this circuit when the impedance looking into the transformer is not zero. Figure 16 shows the circuit analyzed.

Gate and drain input signals with 2 V peak-to-peak excursions were used. With Rs negligibly small, the maximum deviation from linearity was 0.5 percent. As the input signals varied, the voltages on the two current busses remained equal but varied by as much as 0.17 V from the reference value equal to the drain input voltage that represents a zero input.

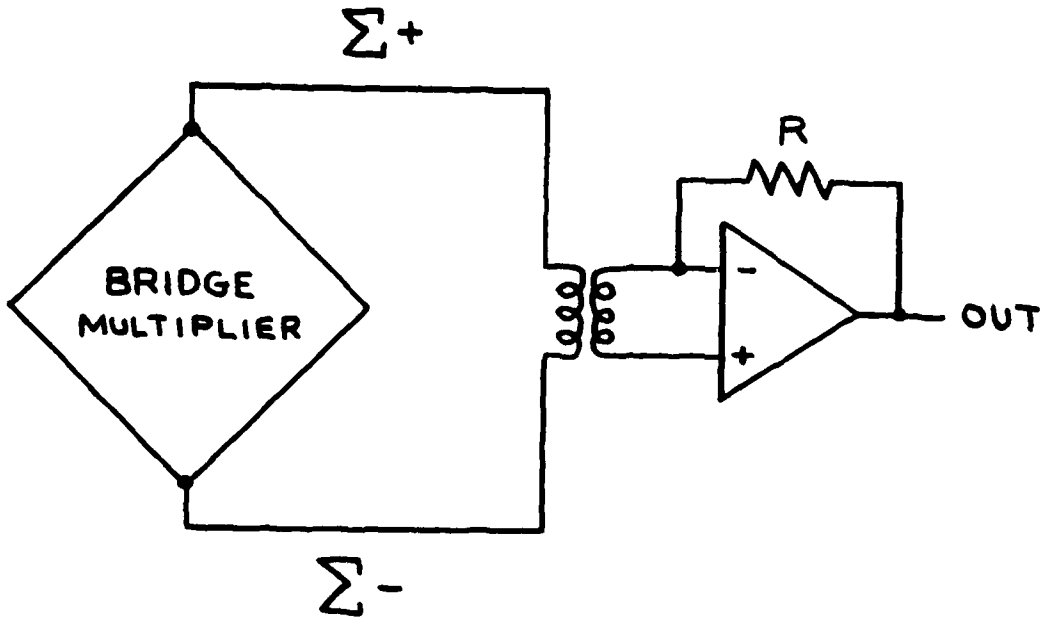

Figure 15. New Technique for Sensing the Differential Current on the Output Current Biases from a Bridge Multiplier

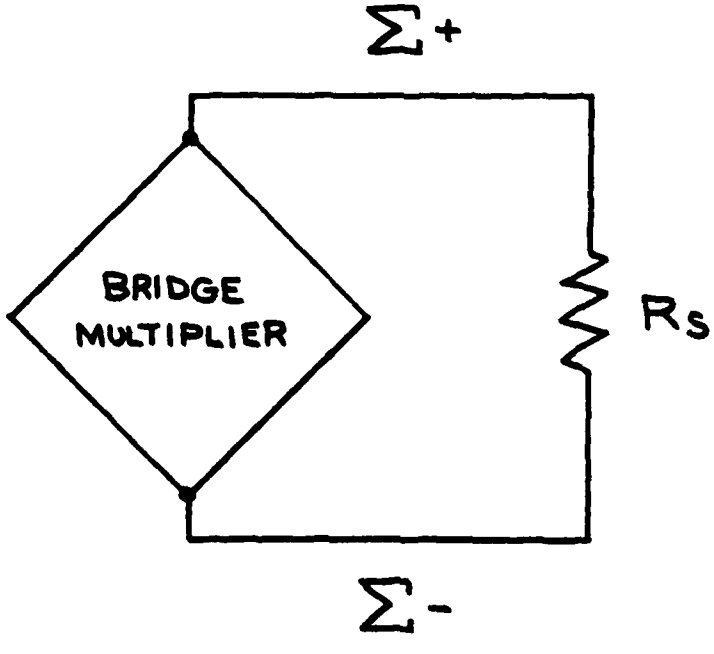

Figure 16. Equivalent Circuit Used for the RAYCAP Simulation

When the sensing impedance was increased to 10 kΩ, a surprising result was found. Although voltage differences as large as 0.1 V (10 percent of the signal amplitude) appeared between the current busses, the maximum deviation from linearity decreased to 0.2 percent. With a 30 kΩ sensing impedance, the maximum bus differential reached 0.22 V, and the peak error reached 0.3 percent. The gain of the multiplier dropped 30 percent. With an extreme sensing impedance of 100 kΩ, the multiplier gain was only about a third of its normal value, the two current busses now had an offset as large as 0.4 V, but the maximum deviation from linearity was still only 1 percent.

4. DESIGN OF THE 526 STAGE CORRELATOR/CONVOLVER

Since the testing of the component parts of the correlator/convolver yielded satisfactory results for the most part, few changes were required in the mask design of the prototype (32-stage version) before the final 256-stage configuration was rendered.

The only changes in the mask design of the correlator stages concerned the locations of interconnect polysilicon and metal routed over the polysilicon gates in the bridge multipliers. As reported earlier, a direct feedthrough of the drain inputs to the multipliers was found to occur in many cases. This feedthrough, which was pattern-related, was investigated and found to be due to a difference in characteristics between those multiplier transistors located under one and under two layers of polysilicon. The double layer of polysilicon was suspected to be providing an extra barrier to the hydrogen anneal cycle. Experiments with lengthened anneal times verified this theory and the decision was made to reroute the second polyinterconnect layer away from the conducting channels in the final design.

It was decided to make all CCDs bidirectional and to provide an extra source-follower-buffered floating gate tap at each end of all CCDs to provide a better assessment of CCD quality and operating conditions.

Additional larger source follower devices were added in series with the floating gate tap source followers to provide the low output resistance needed to drive the package pins and external capacitance loads.

The design of the final version of the correlator was completed and entered into the maskmaking system. Overlays were given final checks and the first masks are expected shortly.

In order to obtain the most uniform threshold and transconductance in the source followers buffering the floating gates and in the multiplier transistors, the maskmaking software was rearranged somewhat. Key exposures of the field oxide and first poly masks were recompiled to insure that the pattern generator would set the outline of critical patterns only once and

then make all the exposures of that pattern before resetting to the next pattern. This will eliminate variations in channel length and width that could occur as a result of variations in the pattern generator aperture setting.

The final chip size is 8.7 mm by a 3.25 mm, and since this is relatively large (as expected), it was decided to have the original correlator/convolver test pattern on the mask series as a dropout in only three locations to maximize yield. The 256-stage device represents one of the first analog integrated circuits that is truly on the scale of a digital LSI device since it contains 4128 CCD cells and 4132 transistors.

5. CONCLUSIONS AND PLANS FOR THE NEXT REPORTING PERIOD

Satisfactory operation has been demonstrated for all the components of the correlator/convolver and operation of a 32-stage test version has shown that these components can be connected to perform together as planned.

The final deliverable 256-stage version of the correlator/convolver has been designed and mask overlays are now being checked in preparation for mask and wafer fabrication. Only two major concerns remain: wafer fabrication defect density, and the matching of offset voltages for the source-follower-buffered floating gate taps.

Defect density is expected to be a problem only because of the relatively large chip area and high complexity level of the completed correlator/convolvers. Although wafer fabrication of the test patterns has proven a high yield of the structures used in the correlator/convolver is possible, all wafer fabrication has been done in a laboratory environment using contact aligners.

If wafer fabrication yields are found to be so low as to preclude the delivery of meaningful best effort samples, additional wafer fabrication can be performed in the Bedford Laboratories wafer fabrication using a projection aligner, automated photoresist equipment, and 3 in. wafers.

The multiplier performance data, the manual measurements on source follower characteristics, and the automated testing of transistor clusters all showed that short-range random variations in parameters such as threshold voltage and transconductance are small enough to meet contract requirements. In a 256-stage correlator/convolver there will in all likelihood be some stages whose inaccuracies exceed the 1 percent goal and others whose accuracy greatly exceeds the requirement. On the whole, observed short-range random parameter variations are consistent with the overall performance desired for the correlator/convolver.

Long-range random or systematic variations are not a problem by virtue of the characteristics of the bridge multiplier. Medium-range random variations, however, can be a problem and, at present, are larger than

desired. Although a small improvement may be obtained using the rearrangement of maskmaking software described above in Section 4, the major sources of these variations are related to the starting material and process parameters.

The variations of offset voltage due to starting material are largely due to the considerable variation in impurity concentration across the wafer. Other sources of offset voltage variation include variations in Q_{SS} and in the work function of the polysilicon gates.

Process experiments will be run during the next reporting period to determine methods to obtain more uniform thresholds and transconductances in devices in future correlator/convolvers. These experiments will concentrate primarily on the following:

1) Use of starting material with more uniform resistivity
2) Obtaining more uniform fixed charge (Q_{SS}) through annealing techniques
3) Achieving more uniformly doped polysilicon

During the next reporting period, the 256-stage correlator/convolver will be fabricated and given final tests prior to delivery of the 20 sample devices and preparation of the final report.

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